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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,570	01/20/2004	Takahiko Murata	60188-754	8016

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EXAMINER

CUTLER, ALBERT H

ART UNIT	PAPER NUMBER
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2622

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/759,570

Applicant(s)

MURATA ET AL.

Examiner

Albert H. Cutler

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is responsive to application 10/759570 filed on January 20, 2004. Claims 1-13 are pending in the application and have been examined by the examiner.

Information Disclosure Statement

2. The Information Disclosure Statements (IDS) mailed on January 20, 2004, July 29, 2005, and February 16, 2007 were received and have been considered by the examiner.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d); which papers have been placed of record in the file.

Specification

4. The disclosure is objected to because of the following informalities: Lack of clarity and precision.

On page 21, line 2, "Each of the other blocks 121 and 122" should be amended to read "Each of the other blocks 122 and 123" in order to preserve clarity. Appropriate correction is required.

Claim Objections

5. Claim 5 is objected to because of the following informalities: Lack of clarity and precision.

Claim 5 recites, "charge signals of pixels including color filters of the same color are sequentially output **and then outputting charge signals.**" Because charge signals of pixels including color filters of the same color are already sequentially output, it is unclear what the aforesaid, "outputting charge signals" is referring to. Please remove "and then outputting charge signals" from claim 1, or include appropriate language to improve clarity. Appropriate correction is required

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 4, 5, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Denyer et al.(U.S. Patent 6,486,911).

Consider claim 1, Denyer et al. teach:

A solid state imaging apparatus(figures 1-6) which includes a plurality of pixels two-dimensionally arranged in the vertical direction and the horizontal direction and in which every two vertically or horizontally adjacent ones of the plurality of pixels includes color filters of different colors(see figure 2, column 5, line 65 through column 6, line 11), the apparatus comprising signal output means(horizontal shift registers 16 and 18, figure 3) for sequentially outputting, in a predetermined period of time(The output is a video signal, column 6, line 67. Video signals are made of images output in a predetermined period of time.), charge signals received from ones of the plurality of pixels including color filters of the same color(column 6, lines 26-55).

Consider claim 2, and as applied to claim 1 above, Denyer et al. further teach:

the signal output means includes means for sequentially outputting, in the predetermined period of time, charge signals received from ones of the plurality of pixels arranged in the horizontal direction and including color filters of the same color(The shift registers are horizontal shift registers(i.e. they output charges from pixels in the horizontal direction). Each shift register sequentially outputs pixels having the same color, column 6, lines 26-55.)

Consider claim 4, and as applied to claim 1 above, Denyer et al. further teach:

the signal outputting means includes a first shift register(16, figure 3) for performing sequential scanning to ones of the plurality of the pixels arranged in the

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horizontal direction(The first shift register sequentially scans pixels of one color, for instance green(i.e. ones of the plurality of pixels arrange horizontally), column 6, lines 42-55.) and a second shift register(18, figure 3) for performing sequential scanning to ones of the plurality of the pixels arranged in the horizontal direction and including color filters of the same color(The second shift register sequentially scans pixels having a color filter of one color, for instance red, column 6, lines 42-55.)

Consider claim 5, and as applied to claim 1 above, Denyer et al. further teach:

the signal outputting means(alternate embodiment, "read out means", 45, figure 6, column 8, lines 30-49) includes a shift register("comprise one or more shift registers", column 8, line 35) for performing sequential scanning to ones of the plurality of the pixels arranged in the horizontal direction(column 8, lines 33-37) and output means(The output means is comprised of the shift register 45, a memory 46, and addressing means 47 and 48, see figure 6.) for switching between a first output method in which charge signals received from the shift register(45) are output so that charge signals of pixels arranged in the horizontal direction are sequentially output(column 8, lines 33-37) and a second output method in which charge signals received from the shift register(A memory circuit(46) receives charges from the shift register, column 8, lines 37-41.) are sequentially output so that charge signals of pixels including color filters of the same color are sequentially output and then outputting charge signals(Charges from color filters of the same color are sequentially output to the main array output, column 8, lines 37-49).

Consider claim 12, Denyer et al. teach:

A camera (figure 4) comprising a solid state imaging apparatus (figures 1-6) which includes a plurality of pixels two-dimensionally arranged in the vertical direction and the horizontal direction and in which every two vertically or horizontally adjacent ones of the plurality of pixels includes color filters of different colors (see figure 2, column 5, line 65 through column 6, line 11), wherein the solid state imaging apparatus includes signal output means (horizontal shift registers 16 and 18, figure 3) for sequentially outputting, in a predetermined period of time (The output is a video signal, column 6, line 67. Video signals are made of images output in a predetermined period of time.), charge signals received from ones of the plurality of pixels including color filters of the same color (column 6, lines 26-55).

8. Claims 6-11, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Saitoh (U.S. Patent 6,377,304).

Consider claim 6, Saitoh teaches:

A solid state imaging apparatus (figure 1, column 8, lines 63-65) comprising:
a plurality of pixels (10, figure 1) two-dimensionally arranged in the row direction and the column direction (column 8, lines 66-67, figure 1);

a sensor section (See figure 1, the sensor section is comprised of the plurality of pixels (10) and their associated circuitry.) for outputting a plurality of selection

signals("pixel outputs", 10, column 9, line 66 through column 10, line 11) so that each of the selection signals(pixel outputs) corresponds to one of a plurality of pixel arrays(Columns. A column of pixels is essentially a one dimensional array, and each pixel output(i.e. selection signal) corresponds to one column.) extending in the column direction in an arrangement of the plurality of pixels(see figure 1);

a first driving circuit for making the sensor section output the selection signals to the pixel arrays so that one of the selection signals for one of the pixel arrays is output at a time(Each of the selection signals(pixel outputs) is output one at a time during the high resolution read-out mode detailed in column 10, line 64 through column 11, line 55. The driving circuit for achieving this read out is also detailed in column 10, line 64 through column 11, line 55); and

a second driving circuit for making the sensor section output the selection signals to the pixel arrays so that ones of the selection signals for plural ones of the pixel arrays are output at a time(Selection signals(pixel outputs) are output two at a time(i.e. ones of the selections signals for plural ones of the pixel array(i.e. columns) are output at a time) in the low resolution readout mode detailed in column 11, line 56 through column 12, line 67. Saitoh also teaches that more than two pixels can be combined, column 12, lines 61-67. The second driving circuit, also detailed in column 11, line 56 through column 12, line 67, uses many of the same components of the first driving circuit. However, it is considered a separate driving circuit because it controls the readout in a different method, by simultaneously connecting multiple readout lines, column 12, lines 12-27.)

Consider claim 7, and as applied to claim 6 above, Saitoh further teaches:

A selection circuit(Horizontal scanning circuit, 22, figure 2, figure 3, column 10, lines 12-62) for selecting a first driving signal sequentially output from the first driving circuit(column 11, lines 28-46) so that the first driving signal corresponds to each of the pixel arrays(Each of the selection signals(pixel outputs) is output one at a time during the high resolution read-out mode detailed in column 10, line 64 through column 11, line 55. The driving circuit for achieving this read out is also detailed in column 10, line 64 through column 11, line 55)) or a second driving signal(column 11, line 61 through column 12, line 18) sequentially output from the second driving circuit so that the second driving signal corresponds to plural ones of the pixel arrays(columns), and then outputting a selected driving signal to the sensor section(Selection signals(pixel outputs) are output two at a time(i.e. ones of the selections signals for plural ones of the pixel array(i.e. columns) are output at a time) in the low resolution readout mode detailed in column 11, line 56 through column 12, line 67. Saitoh also teaches that more than two pixels can be combined, column 12, lines 61-67. The second driving circuit, also detailed in column 11, line 56 through column 12, line 67, uses many of the same components of the first driving circuit. However, it is considered a separate driving circuit because it controls the readout in a different method, by simultaneously connecting multiple readout lines, column 12, lines 12-27.)

Consider claim 8, and as applied to claim 7 above, Saitoh further teaches:

the selection circuit includes a first transistor group(1st stage, 27, figure 3) for outputting the first driving signals to the sensor section so that one of the selection signals(pixel outputs) for one of the pixel arrays(columns) is output at a time(The first transistor group receives a start pulse(ST) and then outputs a drive signal to the sensor section to output one selection signal(pixel output) when the corresponding shift pulse(P1 or P2) is applied. This one selection signal is then output to the horizontal read lines(21S and 21D) shown in figure 1. Column 11, lines 28-46) and

a second transistor group(2nd Stage and 4th Stage, figure 3) for outputting the second driving signals to the sensor section so that ones of the selection signals(pixel outputs) for plural ones of the pixel arrays(columns) are output at a time(The second transistor group receives a start pulse(ST) and then outputs a drive signal to the sensor section to output one selection signal(pixel output) when the corresponding shift pulse(P1 or P2) is applied. However, because control pulses(H1 and H2) are simultaneously switched to high in the low resolution mode, two selection signals(i.e. signals for plural ones of the pixel arrays) are simultaneously read out to the horizontal readout line(21s or 21d), column 11, line 61 through column 12, line 27.)

Consider claim 9, and as applied to claim 8 above, Saitoh further teaches that each of the first(1st Stage) and second(2nd Stage and 4th Stage) transistor groups includes a CMOS transistor(column 10, lines 19-59).

Consider claim 10, and as applied to claim 8 above, Saitoh further teaches that each of the first(1st Stage) and second(2nd Stage and 4th Stage) transistor groups includes an NMOS transistor(column 10, lines 19-59).

Consider claim 11, Saitoh teaches:

A method for driving a solid state imaging apparatus(column 10, line 64 through column 12, line 67) the solid state imaging apparatus(figure 1, column 8, lines 63-65) including a plurality of pixels(10, figure 1) two-dimensionally arranged in the row direction and the column direction(column 8, lines 66-67, figure 1) and a sensor section(See figure 1, the sensor section is comprised of the plurality of pixels(10) and their associated circuitry.) for outputting a plurality of selection signals("pixel outputs", 10, column 9, line 66 through column 10, line 11) so that each of the selection signals(pixel outputs) corresponds to one of a plurality of pixel arrays(Columns. A column of pixels is essentially a one dimensional array, and each pixel output(i.e. selection signal) corresponds to one column.) extending in the column direction in an arrangement of the plurality of pixels(see figure 1), and having a static mode(high resolution mode, column 10, line 63 through column 11, line 55) in which image pickup is performed to a static image("One frame of a video signal(i.e. a static image) is read out at high resolution", column 11, lines 51-55) and a moving image mode(low resolution mode, column 11, line 56 through column 12, line 67) in which image pickup is performed to a moving image(column 12, lines 19-27), comprising:

a first step of outputting, when the static mode(high resolution mode) is selected, the selection signals from the sensor section to the pixel arrays so that one of the selection signals for one of the pixel arrays is output at a time(Each of the selection signals(pixel outputs) is output one at a time during the high resolution read-out mode detailed in column 10, line 64 through column 11, line 55. The driving circuit for achieving this read out is also detailed in column 10, line 64 through column 11, line 55); and

a second step of outputting, when the moving mode(low resolution mode) is selected, the selection signals from the sensor section to the pixel arrays so that ones of the selection signals for plural ones of the pixel arrays are output at a time(Selection signals(pixel outputs) are output two at a time(i.e. ones of the selections signals for plural ones of the pixel array(i.e. columns) are output at a time) in the low resolution readout mode detailed in column 11, line 56 through column 12, line 67. Saitoh also teaches that more than two pixels can be combined, column 12, lines 61-67.)

Consider claim 13, Saitoh teaches:

A camera(solid-state image-pickup device, figure 1) comprising a solid state imaging apparatus(The camera comprises an array of pixels and associated components) which includes:

a plurality of pixels(10, figure 1) two-dimensionally arranged in the row direction and the column direction(column 8, lines 66-67, figure 1);

a sensor section(See figure 1, the sensor section is comprised of the plurality of pixels(10) and their associated circuitry.) for outputting a plurality of selection signals("pixel outputs", 10, column 9, line 66 through column 10, line 11) so that each of the selection signals(pixel outputs) corresponds to one of a plurality of pixel arrays(Columns. A column of pixels is essentially a one dimensional array, and each pixel output(i.e. selection signal) corresponds to one column.) extending in the column direction in an arrangement of the plurality of pixels(see figure 1).)

a first driving circuit for making the sensor section output the selection signals to the pixel arrays so that one of the selection signals for one of the pixel arrays is output at a time(Each of the selection signals(pixel outputs) is output one at a time during the high resolution read-out mode detailed in column 10, line 64 through column 11, line 55. The driving circuit for achieving this read out is also detailed in column 10, line 64 through column 11, line 55); and

a second driving circuit for making the sensor section output the selection signals to the pixel arrays so that ones of the selection signals for plural ones of the pixel arrays are output at a time(Selection signals(pixel outputs) are output two at a time(i.e. ones of the selections signals for plural ones of the pixel array(i.e. columns) are output at a time) in the low resolution readout mode detailed in column 11, line 56 through column 12, line 67. Saitoh also teaches that more than two pixels can be combined, column 12, lines 61-67. The second driving circuit, also detailed in column 11, line 56 through column 12, line 67, uses many of the same components of the first driving circuit. However, it is considered a separate driving circuit because it controls the readout in a

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different method, by simultaneously connecting multiple readout lines, column 12, lines 12-27.)

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Denyer et al. in view of Takashi(Japanese Patent Abstract of Publication 03-029474).

Consider claim 3, and as applied to claim 1 above, Denyer et al. teach the signal output means includes means for sequentially outputting, in the predetermined period of time, charge signals received from ones of the plurality of pixels arranged in the vertical direction and including color filters of the same color(see claim 1 rationale).

However, Denyer et al. teach that the charge signals come from pixels arranged in the horizontal direction(i.e. horizontal shift registers are used). Denyer et al. do not explicitly teach that the charge signals are received from a plurality of pixels arranged in the vertical direction.

Takashi is similar to Denyer et al. in that Takashi is concerned with the readout of a picture from an image pickup device. Takashi is also similar in that horizontal and vertical(lateral and longitudinal) shift registers are used in the output of the image.

In addition to the teachings of Denyer et al., Takashi teaches that charge signals from the plurality of pixels are output in the vertical direction(see Purpose, Constitution).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to read out charges in the vertical direction as taught by Takashi in the imaging apparatus taught by Denyer et al. for the benefit of preventing a picture taken longitudinally from being displayed laterally(Takashi, Purpose), and thus avoiding presenting the user with a side-ways oriented, displeasing image.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert H. Cutler whose telephone number is (571)-270-1460. The examiner can normally be reached on Mon-Fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571)-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC



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SUPERVISORY PATENT EXAMINER